

REMARKS

The above amendments to the above-captioned application along with the following remarks are being submitted as a full and complete response to the Office Action dated June 15, 2004 (U.S. Patent Office Paper No. 10). In view of the above claims currently on file and the following remarks, the Examiner is respectfully requested to give due reconsideration to this application, to indicate the allowability of the claims, and to pass this case to issue.

Status of the Claims

As outlined above, claims 1- 6, 8 and 11 - 15 are currently pending in this application, wherein claims 7, 9, 10 , 16 and 17 are being canceled without prejudice or disclaimer, while the remaining claims are being amended to more particularly and distinctly claim the subject invention. Applicants hereby submit that no new matter is being introduced into the application through the submission of this response.

Prior Art Rejections

The Examiner acknowledged the Response filed on May 18, 2004 and agreed with our response that the prior art of Yamashita et al. is an invalid prior art reference cited against the invention.

However, the Examiner rejected the claims under 35 U.S.C. § 103 claims 1-2, 4-5 and 8 under 35 U.S.C. § 103 as being unpatentable over Ode et al. (US Application No. 2001/0024183) in view of Kawamoto et al. (US Patent No. 6,023,310).

The Examiner also rejected claims 3, 6 and 11-15 under 35 U.S.C. § 103 as being unpatentable over Ode '183 in view of Kawamoto '310 and further in view of Hamilton et al. (US Patent No. 4,503,494).

Lastly, the Examiner rejected claims 7, 9-10 and 16-17 under 35 U.S.C. § 103 as being unpatentable over Ode '183, in view of Kawamoto '310 and further in view of Chiba et al. (US Patent No. 6,380,918). Applicants strongly but respectfully traverse the Examiner's new rejections set forth above.

The present invention as recited in claim 1 is directed to a display device that incorporates a display element; plural driving circuits; a display control device which transmits display data and a clock signal to the plural driving circuits; and a circuit board which is provided between the display control device and the plural driving circuits and supplies the display data and the clock signal transmitted from the display control device, to each of the driving circuits via a bus line and a clock line in the circuit board. At least one of

the bus line and the clock signal line of the circuit board are formed in a continuous area along a long side direction of the circuit board and being divided into plural lines along the long side direction. The plural driving circuits are arranged at one side of the circuit board. A connector is arranged at counter side of the circuit board arranged at center of the printed circuit board. A plurality of connecting lines are connected to at least one of the bus line and the clock signal line and arranged in perpendicular direction to the at least one of the bus line and the clock signal line, and the divided plural lines are electrically connected to the display control device individually through the connecting lines and connector.

As shown in the Explanatory Drawing A attached hereto, which is Figure 6 of the application, a connection between a display control device and a data bus line or clock signal line is minimized where "at least one of the bus line and the clock signal line of the circuit board being formed in a continuous area along a long side direction of the circuit board and being divided into plural lines along the long side direction".

As noted by the Examiner, the primary reference of Ode '183 does not disclose, teach or suggest "at least one of the bus line and the clock signal line of the circuit board being formed in a continuous area along a long side direction of the circuit board and being divided into plural lines along the long side direction".

Similarly, the secondary reference of Kawamoto '310 also does not disclose such a structure such that it can make up for the deficiencies in Ode '183. Rather, Kawamoto '310 merely discloses repair lines S1 to S8 in its Fig. 1A and Fig. 1B, as shown in the attached Explanatory Drawing B. However, the gate side TCP 3 is arranged toward the left side in the figure. Consequently, the distance from S8 to the gate side PCB 5 is very long and S1 to gate side PCB 5 is very short. This causes an imbalance of signals that is avoided by the structure and features of the claimed invention.

Neither tertiary reference to Hamilton '494 nor Chiba '918 provides and disclosure, teaching or suggestion that makes up for any of the deficiencies in either Ode '183 or Kawamoto '310. In particular, Chiba '918 does not discloses or suggest "a connector arranged at counter side of the circuit board and arranged at center of the printed circuit board".

Consequently, none of the prior art references cited against the claims as currently written, either by themselves or in combination with one another noted above, can either anticipate or render obvious each and every feature of the present invention as claimed. Rather, the present invention as a whole is distinguishable and thereby allowable over the prior art.

Conclusion

In view of all the above, Applicants respectfully submit that certain clear and distinct differences as discussed exist between the present invention as now claimed and the prior art references upon which the rejections in the Office Action rely. These differences are more than sufficient that the present invention as now claimed would not have been anticipated nor rendered obvious given the prior art. Rather, the present invention as a whole is distinguishable, and thereby allowable over the prior art.

Favorable reconsideration of this application as amended is respectfully solicited. Should there be any outstanding issues requiring discussion that would further the prosecution and allowance of the above-captioned application, the Examiner is invited to contact the Applicant's undersigned representative at the address and phone number indicated below.

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October 15, 2004